ABSTRACT

A DRAM including an array of storage elements arranged in lines and columns, and for each column: write means adapted to biasing at least a selected one of the elements to a charge level chosen from among a first predetermined high level and a second predetermined low level, combined with read circuitry adapted to determining whether the stored charge level is greater or smaller than a predetermined charge level; and isolation circuitry adapted to isolating the array from the read and/or write means, each column further including refreshment means, distinct from the read and write circuit, for increasing, beyond the first and second predetermined levels, the charge stored in a storage element.